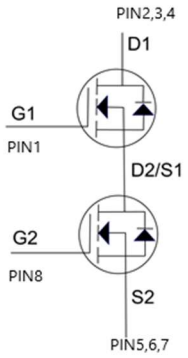
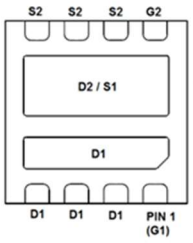
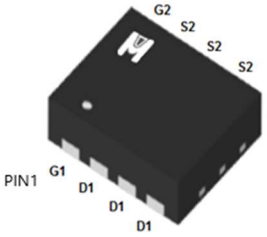
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
V_{DSS}	30V	30V
$R_{DSON\ (MAX.)}$	9mΩ	9mΩ
I_D	16A	16A







N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	16	16	A
	T_C = 100 °C		12	12	
Pulsed Drain Current[1]		I_{DM}	64	64	
Avalanche Current		I_{AS}	16	16	
Avalanche Energy	L = 0.1mH, R_G=25Ω	E_{AS}	12.8	12.8	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	6.4	6.4	
Power Dissipation	T_C = 25 °C	P_D	25	25	W
	T_C = 100 °C		10	10	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
Junction-to-Case	$R_{\theta JC}$	Steady State		5	5	°C / W
Junction-to-Ambient	$R_{\theta JA}$	Steady State		90	90	
	$R_{\theta JA}$	t ≦ 10 s		50	50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≦ 1%

$R_{\theta JA}$ when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	30			V
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1.2	1.8	2.5	
			Q2	1.2	1.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	16			A
			Q2	16			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	Q1		7.7	9	mΩ
		V_{GS} = 10V, I_D = 13A	Q2		7.7	9	
		V_{GS} = 4.5V, I_D = 10A	Q1		11	13	
		V_{GS} = 4.5V, I_D = 10A	Q2		11	13	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 13A	Q1		18		S
		V_{DS} = 5V, I_D = 13A	Q2		18		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q1		959		pF
			Q2		959		
Output Capacitance	C_{oss}		Q1		138		
			Q2		138		
Reverse Transfer Capacitance	C_{rss}		Q1		83		
			Q2		83		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		2.0		Ω
			Q2		2.0		
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DD} = 15V, V_{GS} = 10V, I_D = 13A	Q1		13.7		nC
			Q2		13.7		
	Q_g(V_{GS}=4.5V)		Q1		6.8		

			Q2		6.8		
Gate-Source Charge[1,2]	Q_{gs}	V_{DD} = 15V, V_{GS} = 10V, I_D = 13A	Q1		3.5		
			Q2		3.5		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		2.3		
			Q2		2.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7Ω	Q1		10		nS
			Q2		10		
Rise Time[1,2]	t_r		Q1		15		
			Q2		15		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		Q1		20		
			Q2		20		
Fall Time[1,2]	t_f		Q1		15		
			Q2		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		Q1			16	A
			Q2			16	
Pulsed Current[3]	I_{SM}		Q1			64	
			Q2			64	
Forward Voltage[1]	V_{SD}	I_F = 13A, V_{GS} = 0V	Q1			1.3	V
		I_F = 13A, V_{GS} = 0V	Q2			1.3	
Reverse Recovery Time	t_{rr}	Q1 I_F = 13A, dI_F/dt = 100A / μS	Q1		12		nS
			Q2		12		
Reverse Recovery Charge	Q_{rr}	Q2 I_F = 13A, dI_F/dt = 100A / μS	Q1		14		nC
			Q2		14		

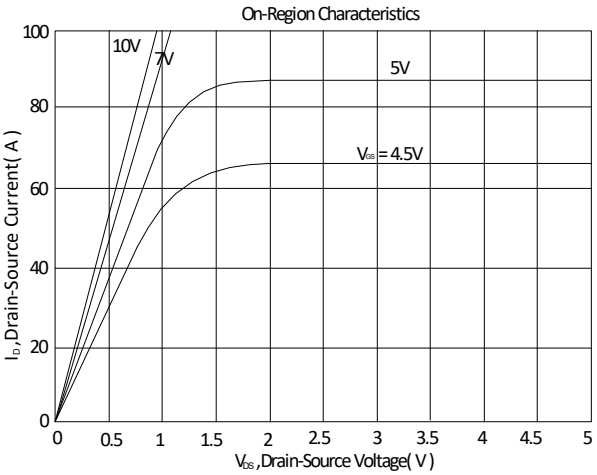
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

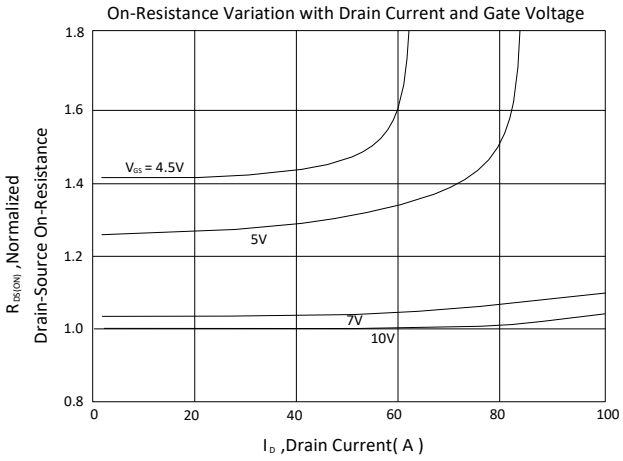
[2]Independent of operating temperature.

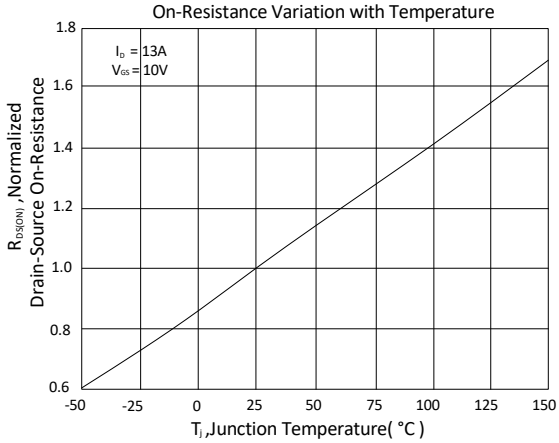
[3]Pulse width limited by maximum junction temperature.

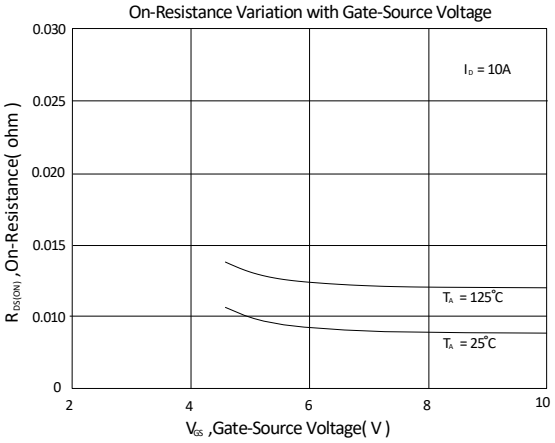
EMC will review datasheet by quarter, and update new version.

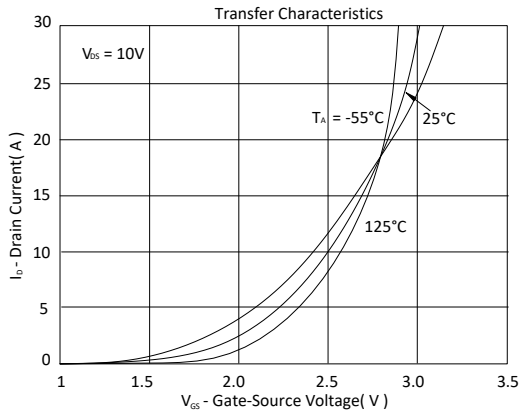
Q1 TYPICAL CHARACTERISTICS

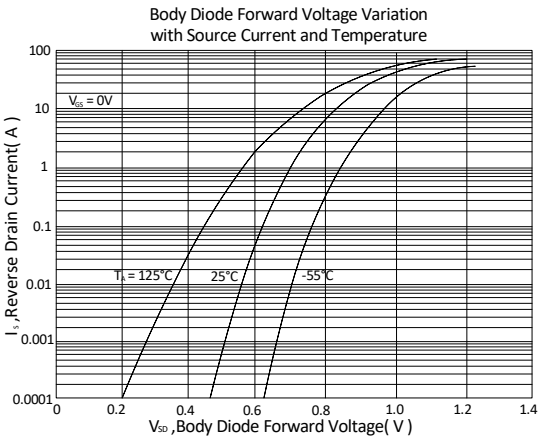


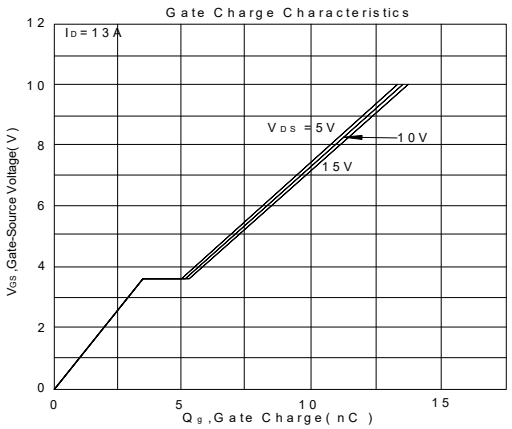


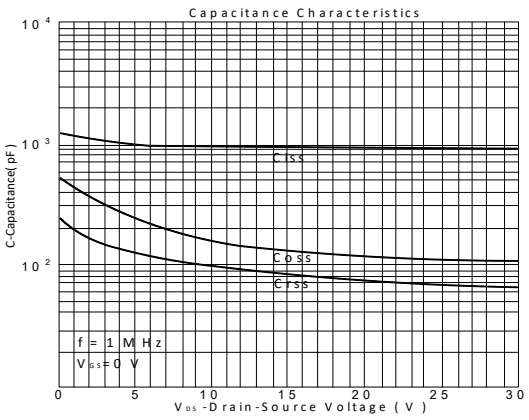


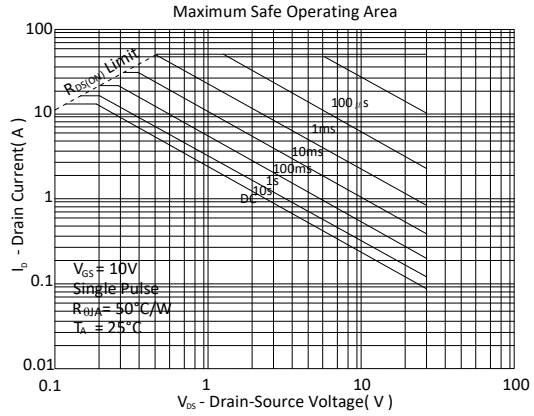


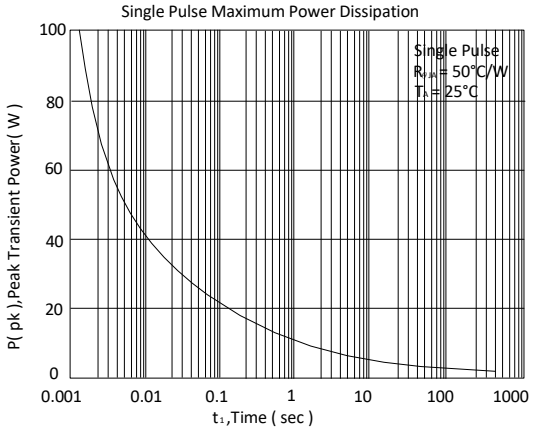


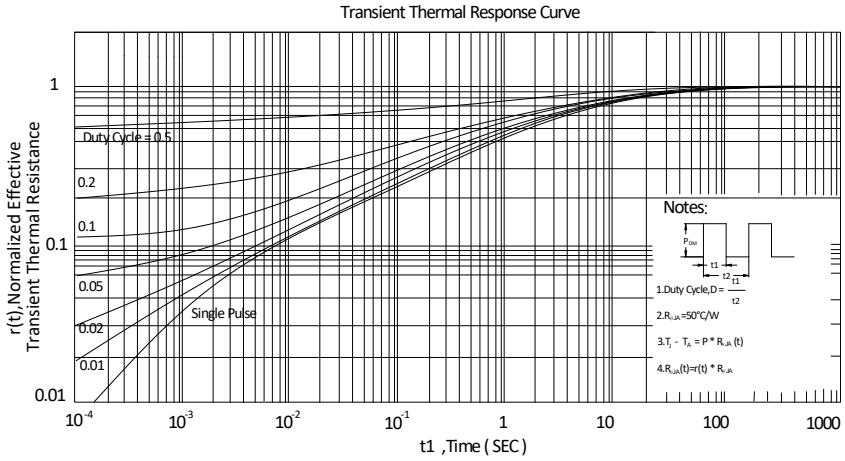



Gate Charge Characteristics
ID = 13 A
VDS = 5 V
10 V
15 V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)

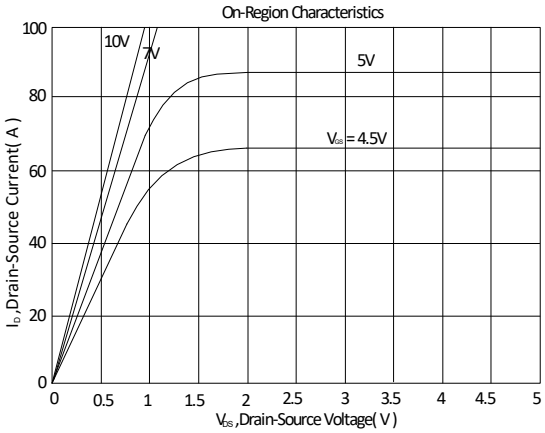

Capacitance Characteristics
Ciss
Coss
Crss
f = 1 MHz
VGS = 0 V
C-Capacitance(pF)
VDS -Drain-Source Voltage (V)

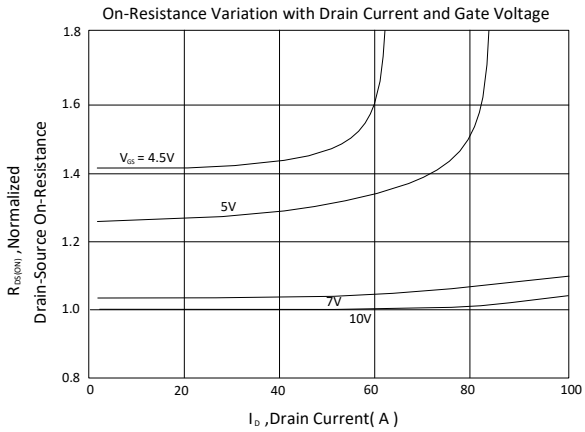

Maximum Safe Operating Area
RDS(ON) Limit
100 μs
1ms
10ms
100ms
1S
DC
VGS = 10V
Single Pulse
RθJA = 50°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)

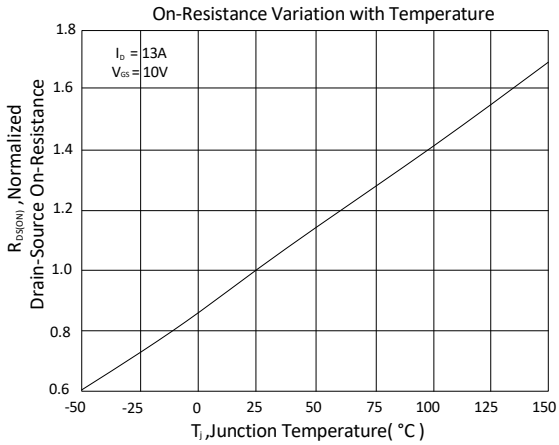

Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 50°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)

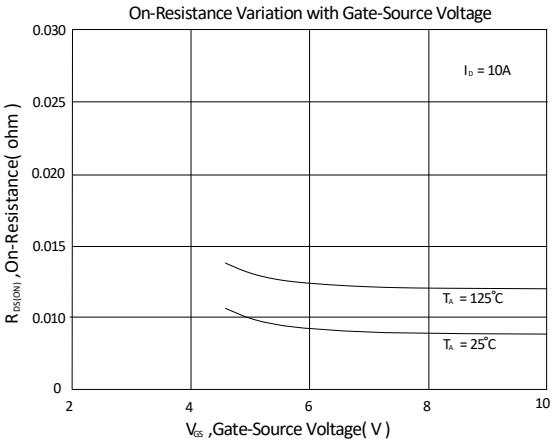

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.RθJA=50°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (SEC)

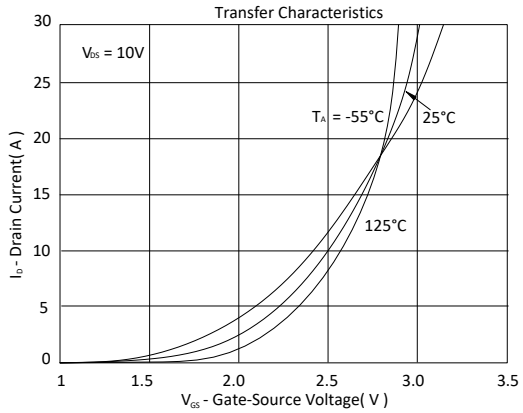
Q2 TYPICAL CHARACTERISTICS

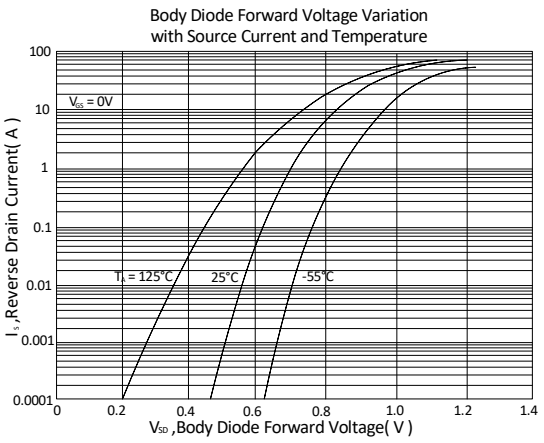


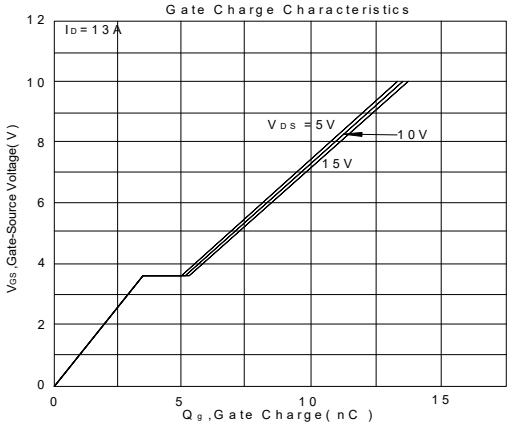








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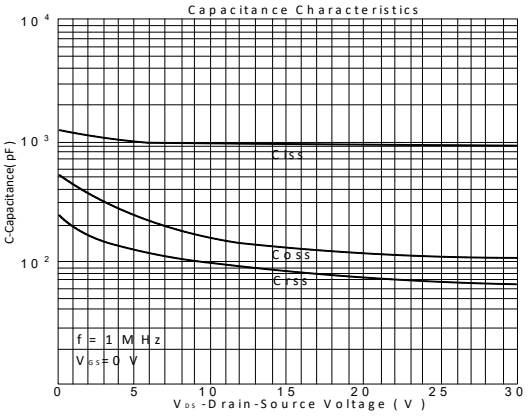
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C-Capacitance(pF)
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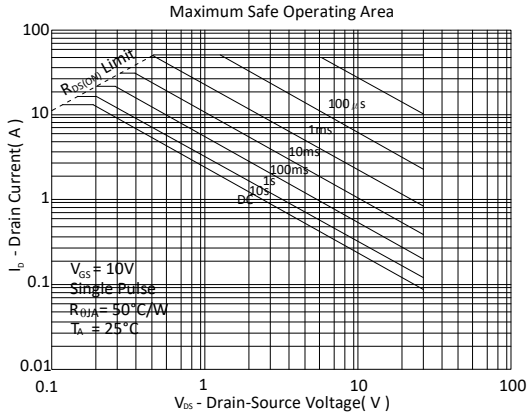
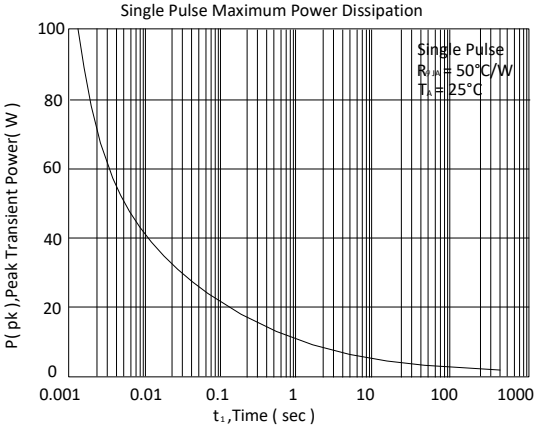
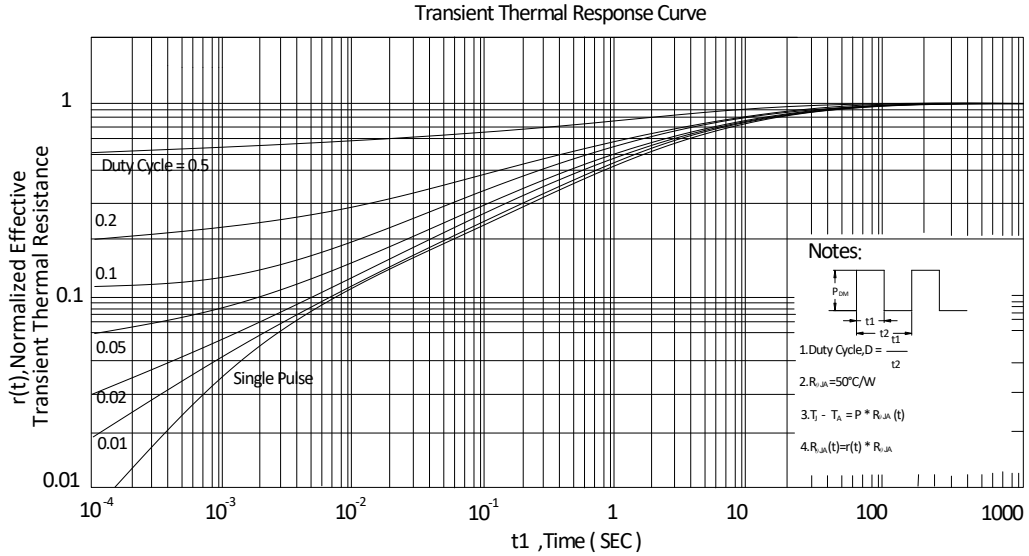
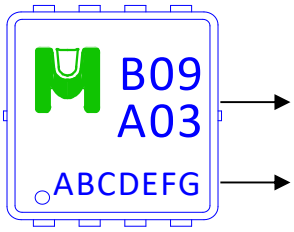

Maximum Safe Operating Area
RDS(ON) Limit
100 μs
1ms
10ms
100ms
1S
10S
DC
VGS = 10V
Single Pulse
RθJA= 50°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 50°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.RθJA=50°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (SEC)

Ordering & Marking Information:

Device Name: EMB09A03VP for Asymmetric Dual DFN3.0X3.0-08



EMB09A03VP: Device Name

ABCDEFG: Date Code

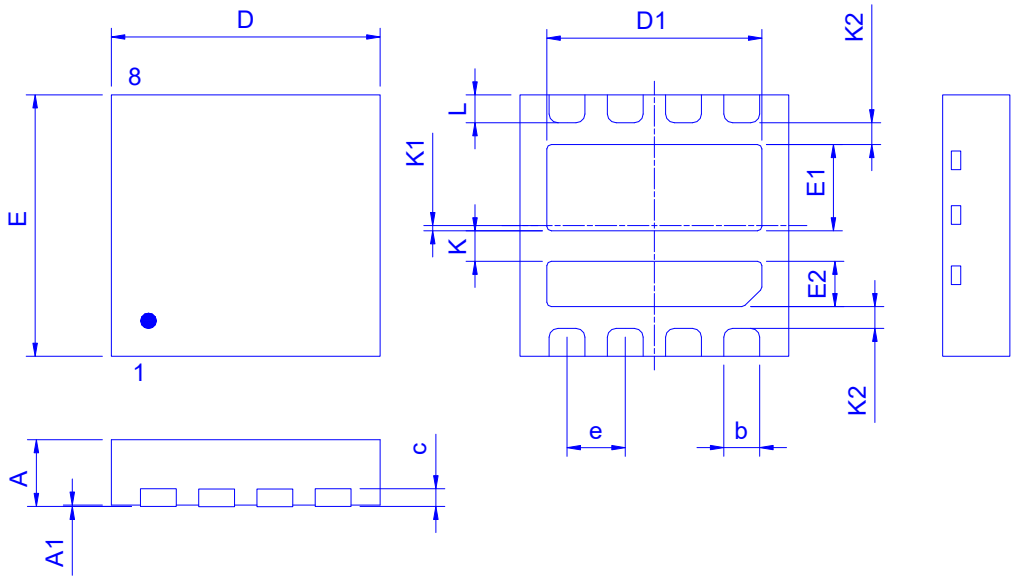
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

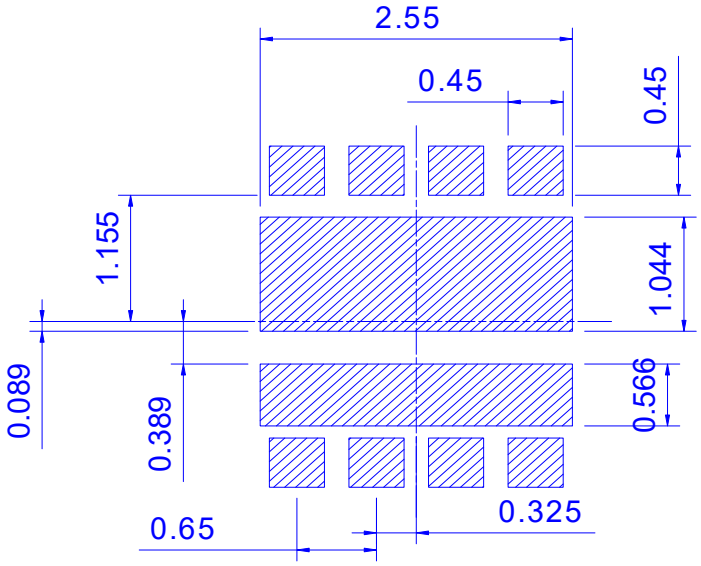
Outline Drawing



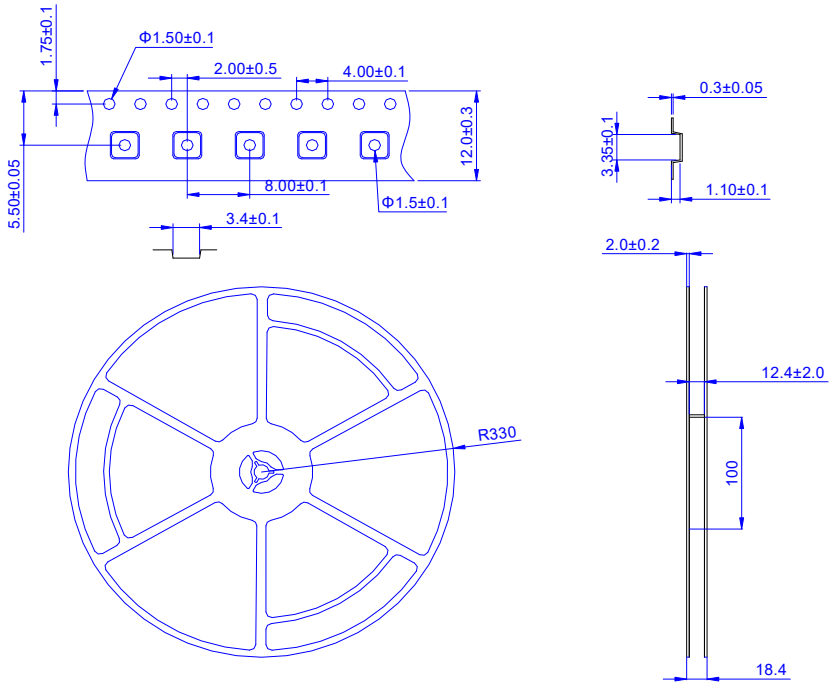
Dimension in mm

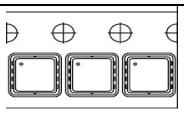
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	K	K1	K2
Min.	0.70	0.00	0.35		2.90	2.30	2.90	0.89	0.42		0.27			
Typ.	0.75		0.40	0.203	3.00	2.40	3.00	0.99	0.52	0.65	0.32	0.35	0.06	0.25
Max.	0.80	0.05	0.45		3.10	2.50	3.10	1.09	0.62		0.37			

Recommended minimum pads



◆ Tape&Reel Information: 5000pcs/Reel



產品別	DFN 3.0X3.0-08
Reel 尺寸	13”
編帶方式	
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1 : 1
內盒滿箱數	5K
內/外箱比	10 : 1
外箱滿箱數	50K